Amendments t the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) A light-emitting thyristor matrix array formed on a chip, comprising:

N (N is an integer ≧ ~~2~~8) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip;

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected;

M (M is an integer ≧ 2) gate selecting lines; and

{(N/M) + M} bonding pads arrayed in one line in parallel with the long side of the chip,

wherein the gate of kth light-emitting thyristor is connected to ith [i ={(k-1) MOD M} +1] gate-selecting line G_i, where "MOD" in an equation means modulo division,

the anode or cathode which is not connected to the common terminal of the kth light-emitting thyristor is connected to jth [j = {(k-i)/M} + 1] anode terminal A_j or cathode terminal K_j,

the number M of the gate-selecting lines is selected so as to satisfy the expression of L/{(N/M) + M}>p (L is a length of the long side of the chip and p is a critical value of the array pitch of the bonding pads) in order to decrease the area of the chip, and

when a prime factor for N is 2 only, the number M of the gate-selecting lines is positive and is the smallest integer, next smaller integer, or third smaller integer that satisfies the expression L/{(N/M)+M}>p.

2. - 5. (Canceled).

6. (Currently Amended) A light-emitting thyristor matrix array formed on a chip, comprising:

N (N is any even integer ~~≧2~~other than 6) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip;

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected;

M (M is an integer ≧ 2) gate-selecting lines; and

{(N/M)+M} bonding pads arrayed in one line in parallel with the long side of the chip,

wherein the gate of kth light-emitting thyristor is connected to ith [i={(k-1) MOD M}+1] gate-selecting line G_I, where "MOD" in an equation means modulo division,

the anode or cathode which is not connected to the common terminal of the kth light-emitting thyristor is connected to jth [j={(k-i)/M}+1] anode terminal A_j or cathode terminal K_j,

the number M of the gate-selecting lines is selected so as to satisfy the expression of L/{(N/M)+M}>p (L is a length of the long side of the chip and p is a critical value of the array pitch of the bonding pads) in order to decrease the area of the chip, and

when prime factors for N are 2 and 3 only, the number M of the gate-selecting lines is positive and is the smallest integer, next smaller integer, third smaller integer, fourth smaller integer, or fifth smaller integer that satisfies the expression $L/\{(N/M) + M\}>p$.

7. (Currently Amended) A light-emitting thyristor matrix array formed on a chip, comprising:

N (N is an integer $\geqq$ ~~2~~8) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip;

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected;

M (M is an integer $\geqq$ 2) anode-selecting lines or cathode-selecting lines; and

{(N/M)+M} bonding pads arrayed in one line in parallel with the long side of the chip,

wherein the anode or cathode of kth light-emitting thyristor is connected to ith [i={(k-1) MOD M} + 1] anode-selecting line A_i or cathode-selecting line K_i, where "MOD" in an equation means modulo division,

the gate of the kth light-emitting thyristor is connected to jth [j={(k-i)/M} + 1] gate terminal G_j,

the number M of the anode-selecting lines or cathode-selecting lines is selected to satisfy the expression of $L/\{(N/M)+M\}>p$ (L is a length of the long side of the chip and p is a critical value of array pitch of the bonding pads) in order to decrease the area of the chip, and

when a prime factor for N is 2 only, M is positve and is the smallest integer, next smaller integer, or third smaller integer that satisfies the expression $L/\{(N/M)+M\}>p$.

8. - 10. (Canceled).

11. (Currently Amended) A light-emitting thyristor matrix array formed on a chip, comprising:

N (N is any even integer ~~≧2~~other than 6) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip;

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected;

M (M is an integer ≧ 2) anode-selecting lines or cathode-selecting lines; and

{(N/M)+M} bonding pads arrayed in one line in parallel with the long side of the chip,

wherein the anode or cathode of kth light-emitting thyristor is connected to ith [i={(k-1) MOD M}+1] anode-selecting line A_i or cathode-selecting line K_i, where "MOD" in an equation means modulo division,

the gate of the kth light-emitting thyristor is connected to jth [j={(k-i)/M}+1] gate terminal G_j,

the number M of the anode-selecting lines or cathode-selecting lines is selected to satisfy the expression of $L/\{(N/M)+M\}>p$ (L is a length of the long side of the chip and p is a critical value of array pitch of the bonding pads) in order to decrease the area of the chip, and

when prime factors for N are 2 and 3 only, M is positive and is the smallest integer, next smaller integer, third smaller integer, fourth smaller integer, or fifth smaller integer that satisfies the expression $L/\{(N/M)+M\}>p$.

12. (Previously Presented) A driver circuit for driving the light-emitting thyristor matrix array according to any one of claims 1 or 6, comprising:

a circuit for driving the gate-selecting lines; and

a circuit for driving the anode terminals or cathode terminals;

wherein the circuit for driving the gate-selecting lines including an even number of gate-selecting signal output terminals and a circuit for outputting a "selecting" signal to one of the gate-selecting signal output terminals and "no-selecting" signal to the others of the gate-selecting signal output terminals, with the terminal to which the "selecting" signal is supplied being switched in turn.

13. (Original) The driver circuit of claim 12, wherein a serial input/parallel output shift register is used for the circuit for driving the gate-selecting lines.

14. (Original) The driver circuit of claim 13, wherein the number of the gate-selecting signal terminals is any one of 4, 6, 8, 12 and 16.